Single Event Latchup Power Switch Cell Characterisation

Vladimir Petrovic, Marko Ilic, Gunter Schoof

Abstract - In this paper are described simulation and measurement processes of a power switch cell used for single event latchup protection of a digital fault tolerant application specific integrated circuit. The standard IHP 250 nm simulation models of components are used for the performed analog simulation using the Virtuoso© Cadence tools.

Keywords - Single event effects, fault-tolerance, power switch, ASIC design methodology

I. Introduction

The development of a design flow methodology for the fault tolerant application specific integrated circuits (ASIC), based on using dual modular redundancy [1] [2], has opened new questions about functional design verification before an ASIC is produced. As it is known, an ASIC can be designed as an analog chip, digital chip or as a mixed-signal chip. The new design methodology [1], is related to production of the fault tolerant ASIC and describes a way how a complex digital ASIC can be designed by using the standard tools in order to provide a digital system resistant to single event effects (SEE). The most known effects in aerospace microelectronics are: single event upsets (SEU), single event transients (SET) and single event latchups (SEL) [4]. The mentioned fault tolerant design methodology is based on using the dual modular redundancy (DMR) instead of using the standard triple modular redundancy (TMR) [3] [8]. The protection against SET and SEU can be done with known techniques on the system level. For the protection against SEL it was necessary to develop new power control circuit.

During the development process of the mentioned new design methodology [1] for a fault free ASIC, we proved that SEUs and SETs can be implemented as fault models into the VHDL code by using standard fault injection methods. The verification of the system functionality, related to the SEU and SET faults is done by the standard digital simulators. From another side, the SEL faults still need to be simulated in analog environment [4]. The basis of this work is verification of the system functionality when a SEL occurs in a digital ASIC and the SEL power switch characterization, in order to provide all needed information for the automated design process [1].

Test designs are implemented in the standard, non-radiation hard IHP's 250 nm CMOS technology [7].

The paper is organized through three sections:

1) Simulation environment of the SPS cell
2) SEL power switch cell description
3) Characterization of the SPS cell

Vladimir Petrovic and Gunter Schoof are with the IHP, Im Technologiepark 25, 15236 Frankfurt Oder, Germany, e-mail: {petrovic, schoof}@ihp-microelectronics.com.

Marko Ilic is with IHP (PhD Student Intern), Klacevica, 35250 Paracin, Serbia, e-mail: markoilic2211@gmail.com.

II. Simulation Environment of the SPS Cell

During the development process of the SPS cell it was important to define an appropriate simulation environment, in order to provide the accurate functional verification. The simulation environment of the SPS cell consists of the three main parts:

a) Latchup generator
b) Control block
c) Digital block supplied by the SPS

In the Fig. 1 is represented the simulation environment, which is also used as a measurement environment for the SPS cell.

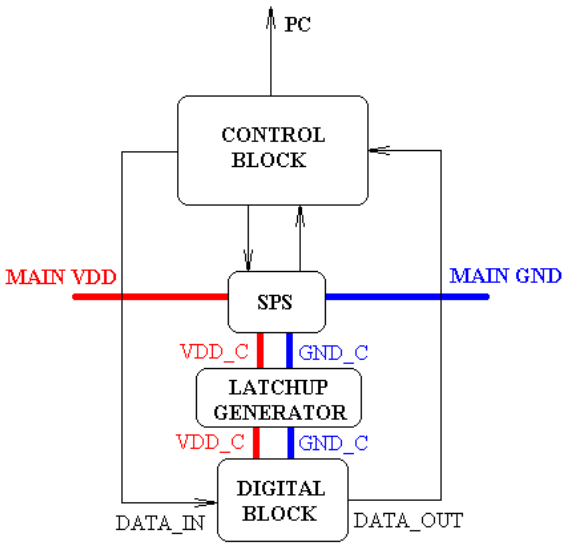

Fig. 1. Simulation environment of the SPS cell

The physical process which describes how a latchup is induced in a CMOS pair is used during the development of the latchup generator. As it is known [4] - [6], the latchup effect is based on a parasitic thyristor component, formed

in the CMOS pair. In order to save the time required for designing a technologically dependent thyristor, a simple switch controlled by voltage (VCSW) is used in the simulation process. This also provides easier hardware realisation of the latchup generator, required for measurements.

The control block is used to provide input control signal of the SPS cell, depended on the output signals generated by SPS cell. The outputs of the SPS are related to the latchup detection and current value of the controlled power supply provided by SPS, while the input signals are controlling the activation of the latchup protection (normal or latchup). The control block is also used for the digital block tests. It provides the stimulus for the digital block during the latchup test. The hardware realisation of the control system is based on the microcontroller system and signal generators.

The digital block, supplied by the SPS cell, is a simple DMR based digital system, which consists of the flip-flops (FF), multiplexers (MUX) and NAND gates. The digital block tests are used to provide information what is exactly happening with the data in the moment when the latchup effect occurs, during and after it. The digital block is implemented in the IHP 250 nm standard cells library.

The simulation process starts by defining the normal operational conditions for the SPS cell, in order to provide the power supply for the digital block. Next step in the simulation process is the digital block validation. The control block provides the data input, clocks and other control signals for the digital block. The control block verifies the correctness of the digital block using the "data out", generated by the digital block. When the digital block is verified, the latchup generator provides a shortcut between VDD_C and GND_C. The VDD_C is controlled voltage supply (VDD) by the SPS and GND_C is controlled ground (GND) line by the SPS (Fig. 1). After the shortcut, the control block should detect a latchup and provide the required control signals in order to test the functionality of the SPS in the latchup mode.

In the next sections of paper are provided the details of the SPS cell functionality, implementation and measurements required for the characterization process. Presented simulation environment is used also as the test environment of the implemented hardware.

III. SEL Power Switch Description

The system protection against single event latchup effect requires design of a special power switch. The SEL power switch cells (SPS) are used in the unity with latchup sensors and power switches for the logic where a latchup was detected. The SPS is a new standard power cell of the IP library [7]. In the design process, the SEL power switch cells should be placed exactly under the power stripes-row crossover points, instead of "filler" cells as usual. The power stripes and power rows at the points where a SPS is placed are connected only through the SPS. In the Fig.2 the power stripes are horizontal power supply lines and the power rows are presented as vertical lines. A SPS has one output – the controlled power supply line, used for one of the redundant circuits. This requirement is based on the concept of having separate power supplies for the two netlists used for the DMR.

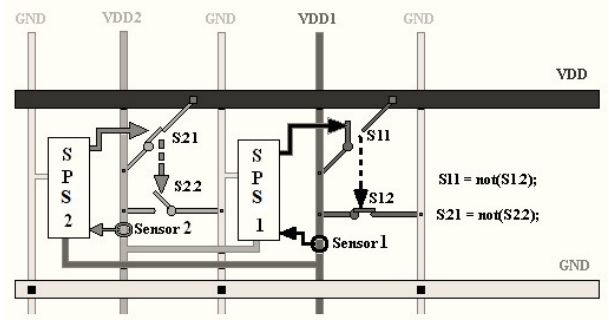

Fig. 2. SEL power switch cells for redundant circuitry

The SPSs, connected on the power supply lines of a redundant circuitry, are presented in Fig. 2. When a latchup is detected, for example on VDD1, the sensor 1 detects much more current then usual and at the same time the drain voltage of the switch S11 decreases to the ground level. Therefore, switch S11 will be opened and switch S12 closed. In this period, when switch S11 is open, the controlled logic is disconnected from the main power supply line VDD1. A sensor is a specially designed transistor for the fast reaction in the latchup handling process. The circuit, where latchup is detected should be disconnected from the main supply line for a period of time defined by control logic (timer or neural network), in order to stop the current flow through the parasitic PNPN structure in CMOS transistor pair, shown in Fig. 3 [A Hastings].

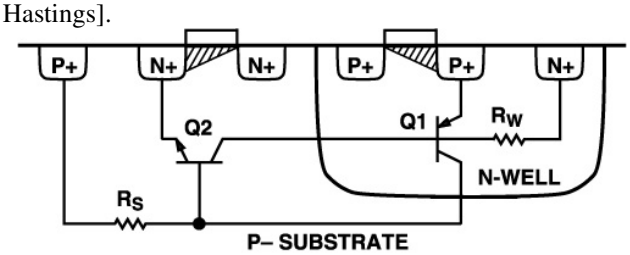

Fig. 3. The parasitic PNPN structure

The redundant circuits are connected to the separated power supply lines - we can call them "domains". As is shown in Fig. 2, SPSs are working in such a way that the SPS, which is connected to one power domain (e.g. VDD1), always controls another power supply domain (e.g. VDD2). This scheme for the power supply connection is done for self-protection of the SPS from the latchup effect. The control logic in a SPS needs to have a continuous and independent power supply in order to make accurate control of the power supply lines for the logic suffering a latchup condition.

In this way, a SPS can react quickly to the latchup and simply makes a disconnection of the harmed part of a system.

IV. CHARACTERIZATION OF THE SPS CELL

A. Introduction

The characterization process of the SPS cell is done through the three main steps. In the development process, the simulation was first important step in order to scale the W/L ratio of the transistors and to provide enough current for the correct functionality of the SPS. The second important step in the characterization process was the implementation of the SPS based circuits. There are three implemented circuit types: the SPS cell, the drive transistors (T5 and T6, Fig. 4) and the SPS cell with small digital system. The measurement was the third important step in the characterization process.

B. Simulation

In Fig. 4 is presented the simplified schematic of the SPS used for simulation. As the SPS cell is used to provide protection on the induced latchup (short-circuit), the simulation (functionality) description is based on this effect.

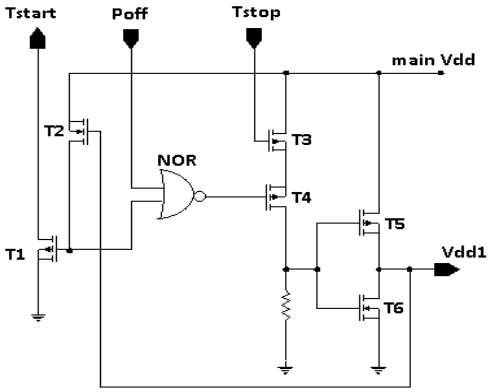

Fig. 4. SPS schematic

In case that output pin Vdd1 is short-circuited, the transistor T5 conducts more current than usual and the voltage between source and drain is higher. That means - the voltage on drain of the PMOS (T5) transistor is being lowered. The time required to set output pin Vdd1 on the zero voltage (ground level) is defined as a power off time (POFT in Fig. 5). Feedback line from the Vdd1 pin causes transistor T2 to activate when mentioned voltage is under the threshold voltage. Automatically, the transistor T1 will trigger Tstart (low active) output pin. Required time to trigger Tstop after latchup is defined as a latchup recognition time (LRT in Fig. 5).

Working condition for the T5 transistors to operate in the linear range and to provide enough current for the digital circuit was one of the most challenging points. From one side, the transistor T5 should be sensitive on the higher current flows, but from another side, the digital system (controlled by the SPS) also has some current fluctuations during the operation time. The solution was to design the transistor which will work on the border between the saturation and the linear range.

In order to wake up the power switch circuit (SPS) from the latchup protection mode, it is required to provide an impulse on the Tstop pin. The minimal length of the Tstop impulse is defined as a minimal activation time (MAT in Fig. 5). This impulse should stop the current flow through the transistor T3 and set the gates of transistors T5 and T6 on the low voltage level. The transistor T5 should activate and provide power supply on Vdd1 output pin. The time required for this process is defined as a power on time (PONT in Fig. 5). The feedback line is deactivating the transistors T2 and T1, where Tstart pin should be set on the high voltage level, whereby latchup protection sequence is finished. The time required for this process is defined as a protection deactivating time (PDT in Fig. 5).

C. Implementation

In order to prove the functionality of the SPS, we have implemented three groups of test circuits in standard IHP 250 nm process [6]. The first group of test circuits is based on the main functionality tests of the SPS and timing measurements in the moment when latchup occurs. The second group of test circuits is used for measuring the burn off time of the output transistor (T5) in the latchup (short-circuit) mode. Transistors are designed with three different W/L ratios – the smallest, middle and the biggest W/L ratio. The third group of test circuits is used for the functional analysis when the SPS cell is integrated in the small digital system.

D. Measurements

Timing measurements are done in order to characterize the SPS as a standard power switch cell for usage in the automated design flow. In Fig. 5 is presented waveform diagram of the mentioned signals and required timings. The strobe signal, in Fig 5, presents the latchup activation signal. The Table I presents simulated and measured signal timings. The timing measurements are done on the 50% voltage level of the signal transitions.

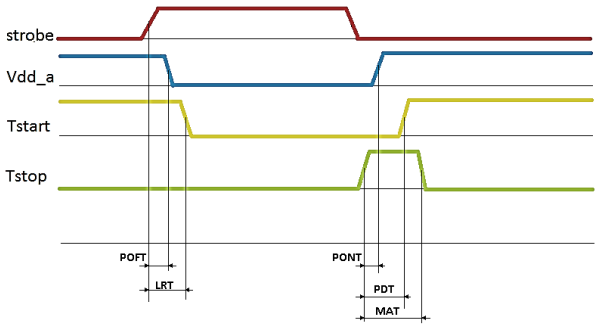

Fig. 5. SPS timing diagram

Before we discuss simulated and measured SPS timings, it is important to note that measurements are done with standard equipment. Measured values are normalized by correction factors for each pad on the test circuit due parasitic capacitances in cables and connections.

TABLE I
SPS TIMINGS (WITH CORRECTED MEASURED VALUES)

	POFT	LRT	PONT	PDT	MAT
Simulated	55.19 [ps]	76 [ps]	487 [ps]	786.5 [ps]	700 [ps]
Measured	120 [ps]	440 [ps]	1.42 [ns]	1.71 [ns]	2 [ns]

It is important also to note that in case of permanent short circuit on the Vdd1 output pin, SPS will automatically be in the protection mode. It is also possible to control activity of the SPS by the Poff pin.

Maximal current tests are based on the longer time shortcut and measurements when the output transistor of power switch cell will be destroyed. The burn off test is done for the output PMOS transistor T5 in order to prove that transistor will survive high current flow in the moment when latchup occurs. Fig. 6 presents the simulation result of the voltage and current for the transistor T5 in the moment when latchup triggers.

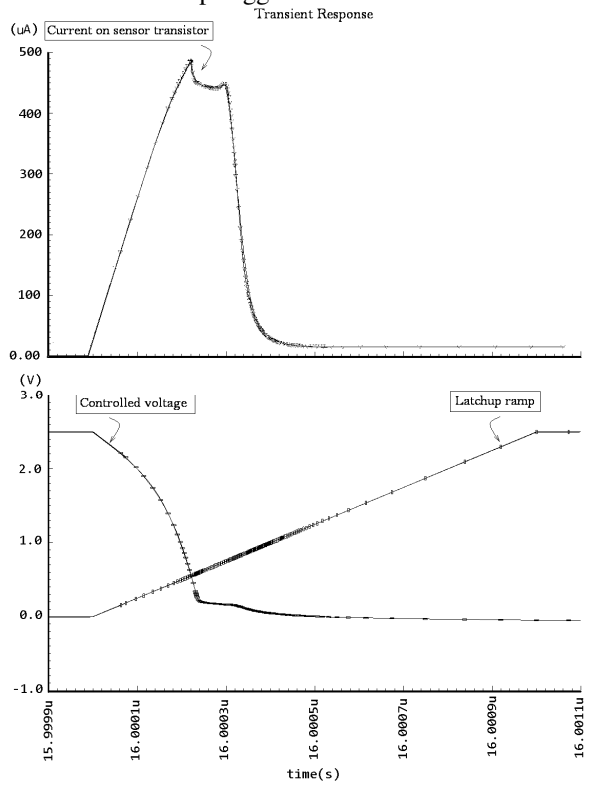

Fig. 6. The current and voltage diagrams after latchup occurrence

In the Table II are presented burn off timings of different test transistors which can be used as transistor T5 (Fig. 4).

TABLE II
BURN OFF TIMINGS (WITH CORRECTED MEASURED VALUES)

W/L	20.83	41.67	208.33
$t_{burn-off}$ [ns]	20	30	38

The measured power consumption, of SPS itself, is about 500 µW in normal conditions and it goes up to 1.25 mW when stimulated latchup occurs. A simulated value of the SPS power consumption is 75 pW in normal conditions and 1.16 mW in the latchup mode. This power consumption difference, between two mentioned modes, is due to the pull-down resistor shown in Fig. 4.

The system used for measurements of the SPS cell, which is integrated in digital circuit is presented in Fig. 7.

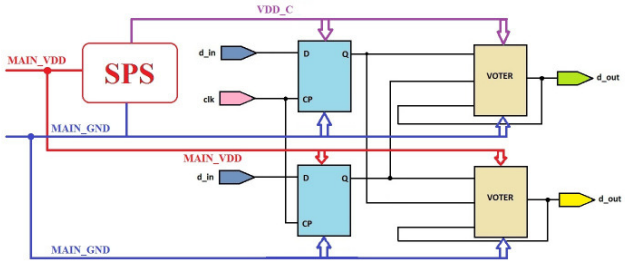

Fig. 7. Digital dual modular redundant circuit with power supply short-circuit protection

After the measurements of the SPS cell, next step was including the protection cell (SPS) in a small digital circuit and testing the functionality when the controlled power supply is short-circuited (VDD_C on Fig. 7). The measurement results are shown in the Fig. 8 [9].

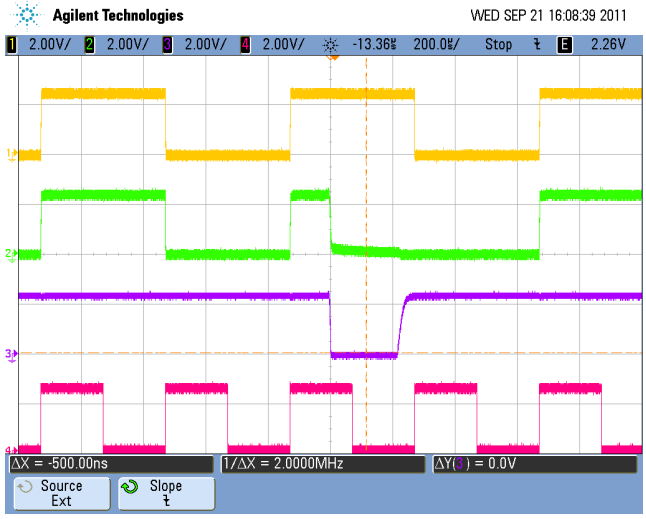

Fig. 8. Measurements of the SPS cell included in digital circuit

In Fig. 8, the third signal presents the power supply line where the latchup is triggered. The second signal in Fig. 8 is the data output of the logic which is supplied by controlled power supply (SPS). The usage of a redundant digital circuit (DMR in this case) provides recovering of the data after latchup is relaxed. From Fig. 8 it is possible

to see that short-circuit protection is active as long as the latchup effect exists.

IV. CONCLUSION

In order to protect an ASIC against SEL effects, we have developed, implemented and tested a custom protection cell – the power switch (SPS).

During tests, we have noticed a problem. The problem is based on the setup time violation in the moment when the latchup protection is deactivated near the active clock edge. Future work will be based on the development of a protection delay and synchronized components in order to avoid such a problem.

It is important to notice that the simulation process of the system with latchup protection still needs to be done in the analog environment in order to verify the complete functionality – the functionality of the digital system and the functionality of the protection system.

The tests of SPS cell, integrated with simple DMR system, have shown correct behave in the latchup period, what provides the adequate usage of the new design flow methodology [1]. The result comparison between simulated and measured values has shown the correctness of the IHP's transistor models used for development and implementation of the SPS cell. The measurement of the SPS driving transistor burn-off time has also shown that during the latchup effect all components in the SPS will not be destroyed.

Further development will be based on the design flow automation for the SPS cells in the layout process and the possibility to implement a neural network for self-testing and control of the power switches (SPS). Radiation tests of described test structures and tests on another technologies (IHP25RH and IHP13) [7] are planned for the next year.

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